FRAGMENT STORAGE FOR DATA ALIGNMENT AND MERGER

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ABSTRACT OF THE DISCLOSURE

[0122] A multiprocessor switching device substantially implemented on a single CMOS integrated circuit is described in connection with a packet data transfer circuit that uses a fragment storage buffer to align and/or merge data being transferred to or from memory on a plurality of channels. In a packet reception embodiment, a data shifter and fragment store buffer are used to align received packet data to any required offset. The aligned data may and then be written to the system bus or combined with data fragments from prior data cycles before being written to the system bus. When packet data is being transferred to memory on a plurality of channels, the fragment storage may be channelized using register files or flip-flops to store intermediate values of packets and states for each channel.